



Attorney Docket No.: 5649-483CTDV

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Seung-Hwan Lee et al.

Group Art Unit: 2823

Serial No.: 10/634,244

Examiner: William D. Coleman

Filed: August 5, 2003

Confirmation No.: 6394

For: INTEGRATED CIRCUIT CAPACITORS HAVING DOPED HSG  
ELECTRODES

September 23, 2004

MS AMENDMENT

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

**REQUEST FOR RECONSIDERATION**

Sir:

The present Request for Reconsideration is in response to the Official Action mailed July 6, 2004. Applicants respectfully submit that all of the claims are in condition for allowance in view of the remarks herein.

It is not believed that an extension of time and/or additional fee(s), including fees for additional claims, are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to our Deposit Account No. 50-0220.

**REMARKS**

Applicants appreciate the thorough examination of the present application that is reflected in the Office Action mailed July 6, 2004. Applicants also appreciate the Examiner's indication that Claims 13 and 14 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. These claims have not be rewritten in independent form because Applicants respectfully submit that all of the pending claims are patentable over U.S. Patent No. 5,943,570 to Park et al. (Park) for the reasons that will now be explained herein.

**Claims 2-8 Satisfy 35 U.S.C. § 112**

Applicants respectfully submit that Claim 5, which recites "further comprising a diffusion barrier layer" has sufficient antecedent basis for "diffusion barrier layer." Claims 2-4 and 6-8 depend from Claim 5 such that their recitations of "diffusion barrier layer" are supported from that claim.

Accordingly, Applicants respectfully request withdrawal of the rejections of those claims under § 112.

**Independent Claim 1 is Patentable Over Park**

Claim 1 recites (emphasis added):

1. An integrated circuit capacitor, comprising:  
a first capacitor electrode on a semiconductor substrate, said first capacitor electrode comprising a conductive layer pattern having a first concentration of first conductivity type dopants therein, and a hemispherical grain (HSG) silicon surface layer on the conductive layer pattern, said HSG silicon surface layer having a second concentration of first conductivity type dopants therein which is greater than the first concentration;  
a dielectric layer on the HSG silicon surface layer; and  
a second capacitor electrode on the dielectric layer.

Accordingly, the concentration of first conductivity type dopants is greater in the HSG silicon surface layer pattern than it is in the conductive layer.

Claim 1 was rejected under 35 U.S.C. § 102(e) as anticipated by Park. In particular, the Office Action contends on pages 2-3 that Park discloses a "conductive layer pattern 14a having a first concentration of first conductivity type dopants therein (column 3, lines 25-27)," and a "HSG silicon surface layer having a second concentration of first conductivity type dopants therein which is greater than the first concentration." However, the Office Action cites to Column 3, lines 30-35 of Park which recites the following (emphasis added):

The first conductive layer may be formed of a polycrystalline silicon film having a first impurity concentration, and the second conductive layer may be formed of an amorphous silicon film having a second impurity concentration which is higher than the first impurity concentration.

The cited portion of Park discloses a capacitor electrode that has two stacked conductive layers, in which one layer has a higher impurity concentration than the other layer, however it does not disclose an impurity concentration of a HSG layer. This stacked electrode structure is shown in FIG. 7 of Park, in which a capacitor electrode is formed by forming a first conductive layer 14 on the insulator 12, and then forming the second conductive layer 16 on the first conductive layer 14. The second conductive layer 16 has a higher impurity concentration than the first conductive layer 14. The first and second conductive layers 14 and 16 are patterned, and then a HSG silicon layer 22 is formed on the stacked first and second conductive layers 14 and 16. (Col. 5, lines 7-34). Although Park discloses the relative concentration of impurities of the first and second conductive layers 14 and 16, it does not disclose an impurity concentration of the HSG layer 22, or much less, how that impurity concentration would compare to the impurity concentration of the first and second conductive layers 14 and 16.

Consequently, Park does not disclose a capacitor electrode with a conductive layer pattern having a first concentration of first conductivity type dopants, and a HSG silicon surface layer pattern that has a second concentration of first conductivity type dopants therein which is greater than the first concentration, as recited in Claim 1.

Accordingly, Applicants respectfully request withdrawal of the rejection of independent Claim 1.

Claims 2-14 are dependent claims and are patentable at least based on the patentability of independent Claim 1.

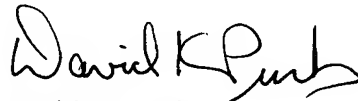
### **Conclusion**

Applicants respectfully submit that the above-entitled application is in condition for allowance. Favorable reconsideration of this application is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite

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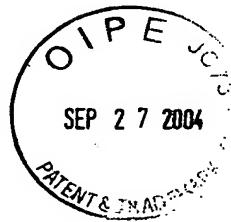
the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



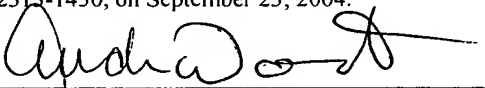
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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MS AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 23, 2004.



Audra Wooten